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SEMICONDUCTOR MEMORY DIAGNOSTIC

reference manual

For HP 1000 M/E/F-Series Computers

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LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the most recent update number on which the technical material on any given page was altered. If a page is simply re-arranged due to a technical change on a previous page, it is not listed as a updated page. Within the manual, changes are marked with a vertical bar in the margin. When a update is incorporated in a reprinted manual, the update number and vertical bar in the margin is removed but the update number will remain on this List of Effective Pages page.

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SECTION I
INTRODUCTION

1-1. GENERAL

The HP 1000 Semiconductor Memory Diagnostic consists of 15 software tests designed to test HP 1000 memory modules for malfunctions associated with semiconductor memories.

Note:

> An additional semiconductor memory diagnostic is available which tests memory via microcode. This diagnostic requires an HP 12978A or HP 13197A Writable Control Store assembly. The absolute binary program number for this diagnostic is 24395-16002; manual part number 24395-90002.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. HP 1000 F-Series, E-Series or M-Series Computer with a minimum of 4K memory.

b. A diagnostic input device.

Any one of the following is optional:

a. HP 12892A/B Memory Protect

b. HP 12976 Dynamic Mapping System for HP 1000 M-Series Computers (memory protect is included)

c. HP 13305 Dynamic Mapping System for HP 1000 E/F-Series Computers (memory protect is included)

1-3. REQUIRED SOFTWARE

The Memory Diagnostic described in this manual is available on one or more media (e.g., paper tape, mini-cartridge tape, disc, and magnetic tape). For the corresponding part numbers associated with these media, refer to appendix A in the *Diagnostic Configurator Reference Manual,* part no. 02100-90157, dated January 1977 or later.

1-4. DIAGNOSTIC SERIAL NUMBER

The Diagnostic Serial Number (DSN) of this diagnostic resides in memory location 126 (octal) except during test sections TST10 and TST16. The DSN is 102104.

PROGRAM ORGANIZATION

SECTION II

2-1. ORGANIZATION

This diagnostic program contains a control section, initialization section, nine standard tests, and six optional tests. The initialization section determines the memory size, options and test options for the main program. A program area check for memory module 0 only is also provided.

2-2. TEST CONTROL AND EXECUTION

The program executes the tests according to the options selected on the S-register by the operator. The program also keeps count of the number of passes that have been completed and will load the A-register with the pass count at the completion of each pass. The count is cleared whenever the program is restarted. Tests are executed one after another in each diagnostic pass.

2-3. SELECTION OF TESTS BY OPERATOR

User selection or default will determine which tests will be executed. The operator may select tests to be executed via S-register bit 9. Paragraph 3-3 outlines the procedures and default tests.

2-4. MESSAGE REPORTING

This diagnostic does not use a console device for reporting errors or providing information. Various halt codes are the sole means of communication with the operator.

2-5. DIAGNOSTIC LIMITATIONS

Memory addresses 0 through 5 are never tested completely.

Refresh tests (TST05 and TST15) can only detect failures in the program area through parity error detection and therefore will not detect errors involving an even number of bits.

The diagnostic will not detect incorrectly configured memory modules. It will, however, display the base memory size it determined in the initialization section to the S-Register for operator confirmation.

Intermittent memory failures are not in all cases identifiable. There have been memory failures in which two successive reads from the same location would give different results. The diagnostic has routines to minimize the chances of incorrectly reporting an error of this nature, but cannot guarantee it.

The default set of program options assumes the minimum operational hardware and that any potential memory failures are hard failures.* The optional tests, many with lengthy execution times, are useful in detecting soft failures.

If the memory protect option is not present, the diagnostic cannot programmatically determine if a main memory or parity chip has failed. The operator must perform the special procedure shown in figure 3-2.

In this diagnostic, memory itself is suspect and, as a result, the program contains a number of irrecoverable halts. These halts and subsequent operations are listed in table 4-1. In TST16 recovery back to program control in all cases is not guaranteed.

TST16 (DMS test) requires a minimum of 36K of memory.

A parity error in the relocating test (TST07) can cause the program to be destroyed.

Some additional limitations apply if the computer contains only 4K of memory: TST10 (module 0 test) will be executed, if selected; however the test will only execute once and destroy the program. The remaining tests will not be executed.

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* A hard failure is defined as a failure which every test will detect. A soft failure is one which only a specific test (usually TST11) or tests will detect.

OPERATING PROCEDURE

SECTION III

3-1. OPERATING PROCEDURE

A flowchart of the operating procedures is provided in figure 3-1.

3-2. TEST SELECTION

The control portion of the program allows the operator to select the tests to be run as follows:

Set S-register bit 9 to indicate that a selection is desired and press RUN. The computer will halt 102075 (T-register contains 102075), indicating it is ready for the test selection. If the program is running, the test in progress will be completed and then the program will halt.

Load the A-register with the tests desired, as defined in table 3-2, and press RUN to execute the selected tests. If the A-register is cleared (or is not set on the first pass) the default tests TST00 through TST10 will be executed.

3-3. RUNNING THE DIAGNOSTIC

The program options are listed in table 3-1. The program will determine the memory size, display the last word of memory address in the Switch Register for a few seconds, restore the program options to the S-register, and proceed with execution. The program will loop with the S-Register, E-Register, and O-Register flashing if memory protect cannot be turned off under program control.

When a halt occurs, refer to table 4-1 for halt definition.

At the completion of each pass of the diagnostic, the pass count is output to the A-register for operator information. If S-register bit 12 is clear, the computer will halt 102077. To run another pass, press RUN. S-register bit 12, if set, is used to loop on the diagnostic; bit 13 is used to loop on a given test that is running at that time. If S-register bit 15 is set, the computer will halt 102076 at the completion of each test.

To enter new memory test limits, set S-register bit 0; the computer will halt 102064 at end of the current test. Enter the new lower and upper memory test limits within base memory in the A- and B-registers, respectively. This feature cannot be used in expanded memory (TST16).

If a trap cell halt 106077 occurs, the user must determine the cause of the interrupt. The diagnostic does not turn on the interrupt system; if an interrupt is caused by a hardware malfunction, the M-register displays the interrupting I/O device select code. The diagnostic may need to be reloaded to continue.

If memory protect is not present, special procedures must be followed to differentiate between main memory and parity chip failures. Error halts can occur by halting on parity error or as a data error halt with an associated halt code. Figure 3-2 illustrates the special procedures to follow for handling errors without memory protect.

The Dynamic Mapping Test in TST16, if selected, will automatically execute all other selected tests on expanded memory after base memory has been tested. The maximum page number determined by this test will be displayed in the S-register for a few seconds when TST16 is selected. The physical memory must be installed in contiguous pages. Testing will start on memory immediately above the first 32K of memory (base memory). TST16 uses the system map only.

The program may be set in a continuous test mode by setting bit 5 of the S-register. In this mode, the program will store non-fatal errors above address 17777 in an error table rather than halting on errors. See table 3-3 for an explanation of the error table.

3-4. PROGRAM AREA CHECK

The initial program area is defined as memory addresses 1000 through 7777. If there is a failure in this area and this area and the program cannot be executed, a Program Area Check of the program area may be executed. (See paragraph 4-18.) The Program Area Check is a separate diagnostic which checks the initial program area. It resides in memory addresses 131 through 677 (octal) and cannot be executed in conjunction with any combination of TST00 through TST14. To execute the Program Area Check, set S-register bit 2, as shown in figure 3-1.

If there are memory failures in the areas where the diagnostic or the Program Area Check test reside, reconfigure the memory modules (making the bad module 2 or 3, etc.), move another module down to module 0, then rerun the diagnostics. If only 4K of memory is present, this diagnostic cannot locate failures distributed throughout module 0.

After the Program Area Check has been executed, the entire diagnostic must be reloaded in order to rerun the diagnostics. Conversely, after the diagnostic test has been executed it must be reloaded to run the Program Area Check. If the total memory size is 4K, the Configurator must also be reloaded.

3-5. TROUBLESHOOTING PROCEDURE

The recommended procedure for using this diagnostic on a suspect memory is to run the default tests (TST00 through TST10) to look for hard failures. Then, if there were no errors, select the desired optional tests to locate any soft failures.

3-6. RESTARTING

The program may be restarted by loading the S-register with the desired program options per table 3-1, set the P-register to 100 or 2000 (octal), and press PRESET, RUN. See figure 3-1. The program may not be restarted, however, when the initialization section, TST07, or TST10 have been aborted.

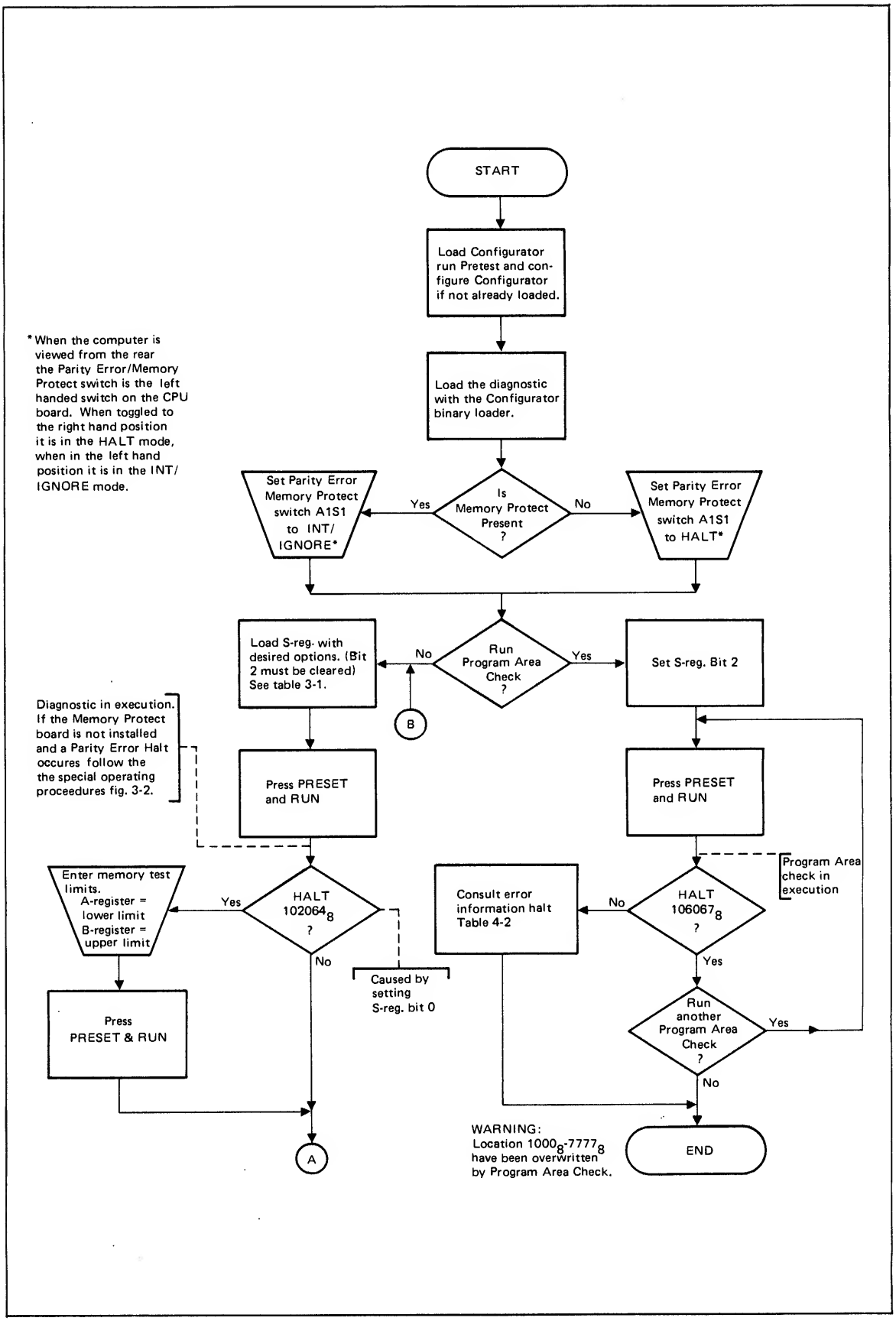


Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)

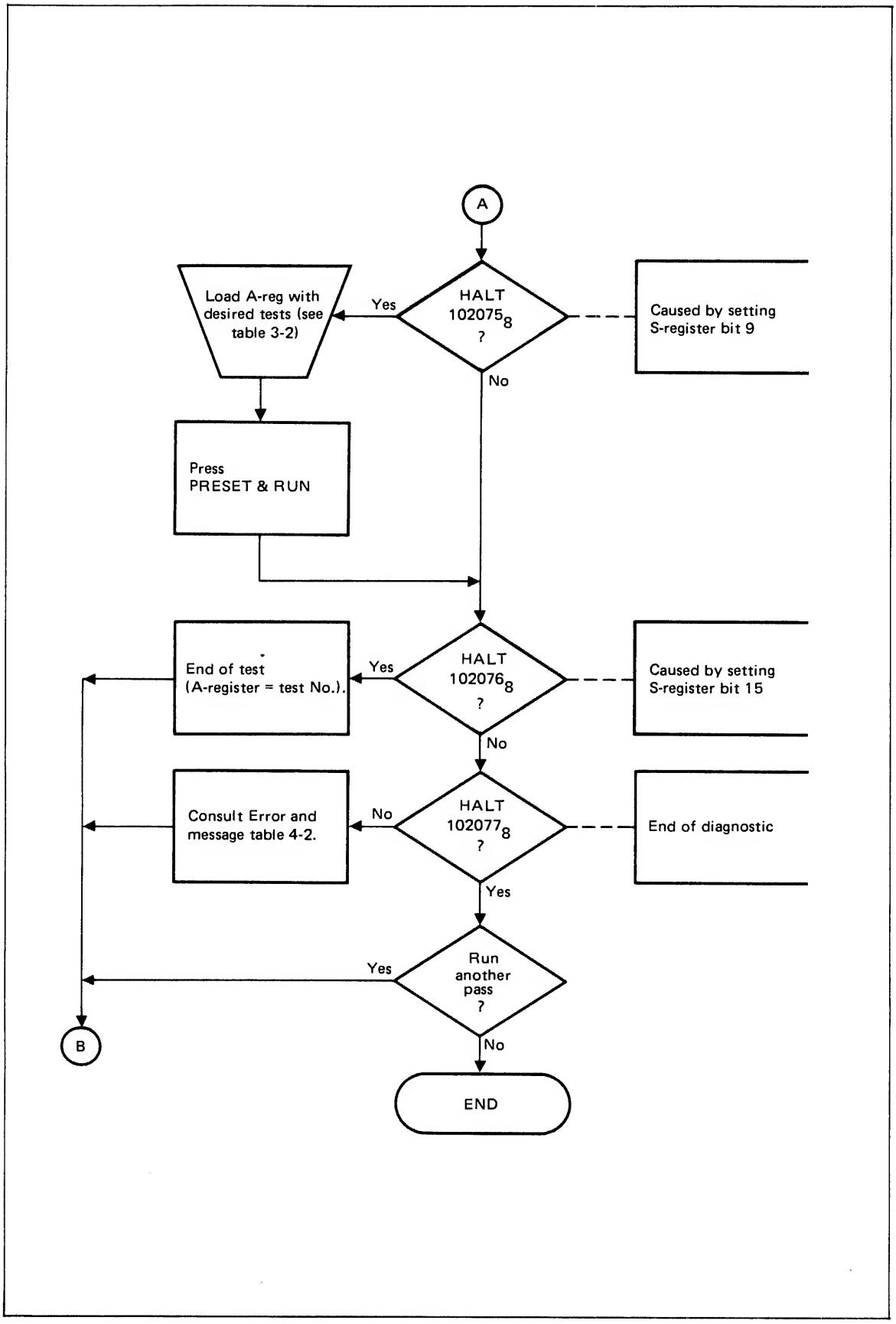


Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 2)

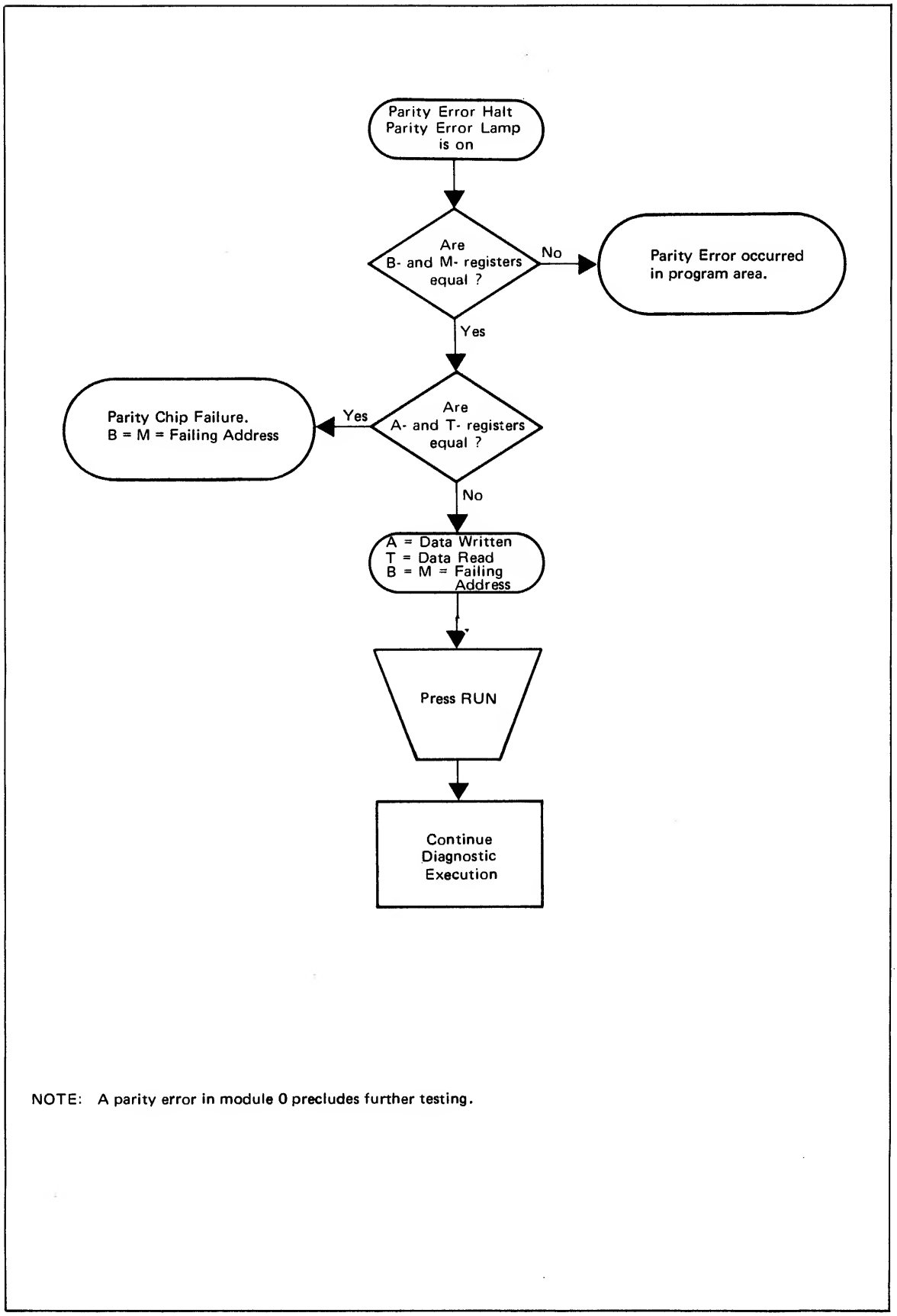
Table 3-1. Program Options

SWITCH-REGISTER BIT	MEANING IF SET
0	Abort execution at end of current test and halt 102064_8 to enter new test limits (must be less than 32K of memory).
1	Reserved.
2	Run Program Area Check.
3	Reserved.
4	Reserved.
5	Store nonfatal errors occurring above address 17777_8 in the Error Table instead of halting.
6	Reserved.
7	Reserved.
8	Suppress operator intervention.
9	Abort diagnostic execution at end of current test section and halt 102075_8. User may specify a new group of tests in the A-register (see table 3-2). Press RUN.
10	Reserved.
11	Reserved.
12	Loop on all selected tests. Tests requiring operator intervention are skipped.
13	Loop on current test section.
14	Suppress error halts.
15	Halt 102076_8 at the end of each test section; the A-register will contain the test number in octal.

Table 3-2. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	TST00 — Ones and Zeros Test.
1	TST01 — Address Parity Test.
2	TST02 — Marching Ones and Zeros Test.
3	TST03 — Checkerboard Test.
4	TST04 — Rows and Columns Test.
5	TST05 — Disturbance Test.
6	TST06 — Diagonal Test.
7	TST07 — Relocating Test.
8	TST10 — Module 0 Test.
9	*TST11 — Galloping Read Recovery Test.
10	*TST12 — Lonely Bit Test.
11	*TST13 — Extended Instruction Group Test.
12	*TST14 — Memory Protect Test.
13	*TST15 — Intervention Refresh Test.
14	*TST16 — Dynamic Mapping System Test.
15	Reserved.
B-Register	Reserved.

*TST11 through TST16 are optional tests and must be selected via test selection. See paragraph 3-3. The default set or clearing the A-register will result in execution of TST00 through 10. If bit 14 is set, all other selected tests will be performed on base memory, then all selected tests will be executed as subtests of TST16 in expanded memory. If only bit 14 is set, the default tests TST00 through TST10 will be performed on base memory, then on expanded memory. Anytime TST16 is executed, the maximum page number will be displayed in the switch-register as soon as execution is initiated.



NOTE: A parity error in module 0 precludes further testing.

Figure 3-2. Special Procedures for Handling Parity Errors Without Memory Protect

Table 3-3. Error Table

If Switch-register bit 5 is set, errors which are not fatal to the diagnostic itself, and are located above 8K will be stored in a table beginning at location 1600_8. Error entries will be limited to one error per 4K memory module. Additional errors within that 4K memory module will be ignored. Each error will occupy five consecutive memory locations in the error table. The first location holds either a 15_{10} bit base memory address ($\geq 20000_8$) or a 10_{10} bit page address in expanded memory. The second contains the data written. The third location contains the data read. The fourth location contains all ones for base memory failures or the page number for errors in expanded memory. The last location holds the number of times (maximum of 65K) an error has occurred at this address.

Individual Error Entry Format:

M = Address of Error (15_{10} bit address in base memory or 10_{10} bit page address in expanded memory)
M+1 = Data Written
M+2 = Data Read
M+3 = 177777_8 in base memory or page number in expanded memory
M+4 = Number of times an error occurred at this address

The distribution of error entries in the table depends on the presence of DMS. If DMS is present, errors may be distributed in any order in the error table and the entries must be individually analyzed to determine their physical location in memory. If any module's table locations are full (4 errors in 4 separate 4K modules with DMS), a fifth error in a fifth 4K module will halt. An Error Table Summary is also provided.

Error Table*

Error Table for Base Memory			Error Table for Base and Expanded Memory		Location Containing the Number of Errors (Maximum of 4) Entered in the Corresponding Error Table Locations
Module Number	**Addresses in Module**	**Error Table Locations**	**Page Numbers**	**Error Table Locations**	
2	20000-27777	1600-1604	10+(N)(30) ** thru 13+(N)(30) **	1600-1623	1770
3	30000-37777	1624-1630	14+(N)(30) ** thru 17+(N)(30) **	1624-1647	1771
4	40000-47777	1650-1654	20+(N)(30) ** thru 23+(N)(30) **	1650-1673	1772
5	50000-57777	1674-1700	24+(N)(30) ** thru 27+(N)(30) **	1674-1717	1773
6	60000-67777	1720-1724	30+(N)(30) ** thru 33+(N)(30) **	1720-1743	1774
7	70000-77777	1744-1750	34+(N)(30) ** thru 37+(N)(30) **	1744-1767	1775

*All numbers are octal.
**N is an octal integer number such that $0 \leq N \leq 53$ and the page number can be determined by the formulas.

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. TEST DESCRIPTION

The initialization section, Program Area Check and 15 tests in this diagnostic are described in detail in the following paragraphs. A listing of error and information halts is provided in table 4-1. All tests will perform a complement of the pattern used and a parity chip version of the pattern and its complement in each test.

In the initialization test section, the program will be moved within memory module 0 or to different areas of module 1. This will result in module 0 containing data patterns in some phases of testing instead of program object data. Due to these facts, the (DSN) may be located at address 10126 (octal) or 1126 (octal) rather than location 126 (octal).

4-2. INITIALIZATION SECTION

The initialization section primarily determines parameters for the diagnostic. These parameters are: memory size, memory protect option, and basic workability of the program area. The memory size and option sections are overlayed upon completion and cannot be reused. To rerun those sections, the diagnostic must be reloaded. To minimize memory configuration errors, this section will display the calculated memory size found in the S-register for a few seconds. The operator visually verifies that the value displayed is equivalent to the memory configured. The S-register is also tested prior to its use. The remaining memory initialization section moves the program around in the program area to do a quick verification of locations 6 through 7777 (octal) to look for hard failures in that area. These are irrecoverable errors.

4-3. ONES AND ZEROS TEST — TST00

This test section writes/reads each word of memory under test to 000000, 177777, 000001 and 177776 (octal). The last two patterns are shifted 16 (decimal) times to move a one through a field of 15 (decimal) zeros and a zero through a field of 15 (decimal) ones.

4-4. ADDRESS PARITY TEST — TST01

This test section simply writes/reads each cell to the parity of its address. Using odd parity as an example — each word would contain all zeros for an odd number of bits in its address and all ones for an even number of bits in its address. This is done for both even and odd parity.

4-5. MARCHING ONES AND ZEROS TEST — TST02

This test section writes memory to all zeros. Then, starting at the address of lower limit under test, reads all zeros, writes all ones, reads all ones, moves up to next location and repeats this process until through the upper limit of the area under test. Next, the test area is checked for all ones. Now, the process is repeated in descending order and then the test area is again checked for all zeros. The complement pattern is then executed. That is, the memory under test is written to all ones, address of lower limit of memory under test reads all ones, writes all zeros, reads all zeros, moves up to the next location, etc. The parity chips are tested using the data values 000001 (octal) and 177776 (octal) instead of ones.

4-6. CHECKERBOARD TEST — TST03

Main memory and parity chips are written/read to a "checkerboard" pattern and its complement.

4-7. ROWS AND COLUMNS TEST — TST04

Patterns of alternating ones and zeros by rows, then columns, are written/read. The patterns are complemented and then duplicated for the parity chips.

4-8. DISTURBANCE TEST — TST05

This test section writes/reads remaining combinations of opposite polarity around any given cell location on the chip. The patterns are complemented and duplicated for the parity chip.

4-9. DIAGONAL TEST — TST06

These tests write a series of zeros followed by a one, another series of zeros, a one, etc. See for the 8x8 array case. The pattern is then shifted throughout the chip, complemented, and duplicated for the parity chip.

4-10. RELOCATING TEST — TST07

The relocating test is composed of a relocating module and the tests in TST00 through TST03. The relocating test is performed only on the 4K memory modules above module 0. The test section forms a module which relocates up to the next adjacent 4K memory module and tests that module, while residing there, by writing and reading the test patterns in TST00 through TST03. The relocating module then "walks through" and tests each 4K module.

4-11. MODULE 0 TEST — TST10

This test section performs the ones and zeros, address parity, marching ones and zeros, and checkerboard tests on memory module 0 by moving the program as it is tested. Locations 0 through 5 are not tested. Errors here are fatal.

4-12. GALLOPING READ RECOVERY TEST — TST11

This test is simultaneously the most effective and longest test for the current generation of 4K RAM chips. The chip will see a pattern of a one in a field of 4095 zeros or a zero in a field of 4095 ones. The sequence of events is as follows:

a. All locations are written to a background pattern of zeros.

b. Data=zeros are read from all locations.

c. Read cell 0. Should be zero.

d. Write cell 0 to a 1 (this becomes the test cell).

e. Read cell 0. Should be one.

f. Read cell 1. Should be zero.

g. Read cell 0. Should be one.

h. Read cell 2. Should be zero.

i. Read cell 0. Should be one.

   – continue to read each background cell for a zero and then back to the test cell for a one until . . .

j. Read cell 4095. Should be zero.

k. Write cell 0 back to zero.

l. Make the test cell location the next cell in ascending order and repeat tests starting at d.

   – continue reading one to zero on all possible combinations until test cell is 4095 and then finish the last pass on the chip.

m. Repeat entire sequence using a background of ones and a test cell of zero.

n. Duplicate for parity chip.

Due to the fact that all read access combinations are tries in N^2 iterations (where N = memory size), this test is one of the "N-squared" tests. This test has been called "GALPAT" or "PING-PONG".

4-13. LONELY BIT TEST — TST12

This test also uses the same patterns as the Galloping Read Recovery test; however, it is only written/read in ascending order.

4-14. EXTENDED INSTRUCTION GROUP TEST — TST13

This test section uses some instructions from the extended instruction group to write/read memory faster than can be done using memory reference group instructions. The instructions used are MVW (Move Words) and CMW (Compare Words). The instructions will move/compare the checkerboard pattern described in TST03 through the memory under test.

4-15. MEMORY PROTECT TEST — TST14

If memory protect is present, this test will go through the memory under test reading data on both sides of the fence register. This test assumes a working memory protect.

4-16. INTERVENTION REFRESH TEST — TST15

This test writes memory under test to zeros and then halts. The operator then presses RUN, which verifies the written pattern then writes new data. The process is repeated using 000001 (octal) and 177776 (octal). When TST15 is being executed as a subtest of TST16 do not press PRESET, as this will disable the memory maps.

4-17. DYNAMIC MAPPING SYSTEM TEST — TST16

This test runs in conjunction with the Dynamic Mapping System (DMS), if present. The selected tests (TST00 through TST15) are executed as subtests of TST16 on all available memory above 32K. The DMS hardware is assumed operational. Only the system map is used.

4-18. PROGRAM AREA CHECK

If the initial program area (1000 to 7777 (octal)) has memory failures, then the normal diagnostic program may produce unpredictable results. The Program Area Check is located below the initial program area and checks locations 1000 through 7777 (octal). This check is used only to identify errors in that area. It cannot be executed in conjunction with the diagnostic. Execution of the Program Area Check destroys the main diagnostic program and is selected by the special procedure described in paragraph 3-3. Execution time is less than 8 seconds.

Table 4-1. Error and Information Halts

HALT CODE (OCTAL)	TEST SECTION	MEANING
102000	TST00	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102001	TST01	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102002	TST02	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102003	TST03	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102004	TST04	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102005	TST05	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102006	TST06	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102007	TST07	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102011	TST11	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102012	TST12	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102013	TST13	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102014	TST14	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102015	TST15	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.
102016	TST16	Data error. A-register contains the data written and the B-register contains the data read. Press RUN for failing address.

Table 4-1. Error Information Halts (Continued)

HALT CODE (OCTAL)	TEST SECTION	MEANING
102027	ANY	Secondary error halt. A-register contains the failing address (page address if in expanded memory). B-register contains all ones if error is in base memory, or the page number if in expanded memory. Press RUN to continue.
102030	TEST CONTROL	Memory upper limit entered in B-register after halt 102065 is still greater than calculated memory size. Re-enter limit in B-register or leave current value to run tests on memory above calculated size. Press RUN.
102034	ANY	Parity error occurred above address 7777 and the program was not verifying data previously written. A-register contains the failing address (Page address if in expanded memory). B-register contains all ones if address is in base memory or page number if in expanded memory. If in TST07, the test section is aborted. Press RUN to continue.
102035	TST07, TST11, or TST12	Test selected cannot be executed due to test limits not being located on 4K main memory boundaries. Press RUN to go back to enter new test limits.
102036	TEST CONTROL	No expanded memory could be found. Press RUN to return to operator selection.
102060	TST15	Halt to allow memory to refresh itself. Press RUN to continue. Do not press PRESET. Occurs three times consecutively. In TST16, however, this halt may occur any number of times depending on memory size.
102061	ANY	Test selected cannot be run because there is only 4K of memory present.
102062	TST14	Test selected cannot be run because memory protect is not present.
102063	INITIALIZATION or TST07	Data error at destination of a move occurred. A-register contains data written and B-register contains data read. Press RUN to get failing address.
102064	TEST CONTROL	Halt to enter new test limits (less than 32K memory only). Put lower limit in A-register and upper limit in B-register, press RUN.
102065	TEST CONTROL	Memory upper limit entered in B-register greater than calculated memory. Re-enter limit in B-register or leave current value to check above calculated memory. Press RUN.

Table 4-1. Error and Information Halts (Continued)

HALT CODE (OCTAL)	TEST SECTION	MEANING
102066	TEST CONTROL	Memory lower limit entered in A-register is larger than or equal to upper limit in B-register. Correct values and press RUN.
102067	TEST CONTROL	Memory lower limit entered in A-register is below 10000_8. Re-enter limit in A-register and press RUN.
102075	TEST CONTROL	Test selection request resulting from Switch-register bit 9 being set. Enter the desired group of tests to be run into the A-register, and press RUN. See table 3-1.
102076	TEST CONTROL	End-of-test halt resulting from Switch-register bit 15 being set. A-register contains the test number. Press RUN to continue.
102077	TEST CONTROL	Diagnostic pass complete. A-register contains the pass count. To do another pass, press RUN.
106001	ANY	Irrecoverable parity error in module 0. A-and B-register contain the address of the parity error.
106002	ANY	Erroneous memory protect error. Fix problem before restarting.
106004	INITIALIZATION, PROGRAM AREA CHECK, or TST10	Data error in memory module 0 precludes further testing. A-register contains the data written and the B-register contains the data read. Press RUN to obtain the failing address.
106005	INITIALIZATION, PROGRAM AREA CHECK, or TST10	Secondary error halt. A- and B-register both contain the failing address. Irrecoverable.
106010	INITIALIZATION	Memory determination routine wrote all ones and read something other than ones or zeros back. Fix problem and reload or set desired last word of memory address in the B-register and press RUN.
106011	INITIALIZATION	Memory determination routine could not find any memory. Fix problem before proceeding.
106012	ANY	Program destroyed. If available, see listing.
106013	INITIALIZATION	The Switch-register failed. A-register contains the data output to the Switch-register and the B-register contains the data loaded from the Switch-register. Irrecoverable.
106014	INITIALIZATION	Memory protect failed. Run memory protect diagnostic to analyze failure. Irrecoverable.

Table 4-1. Error and Information Halts (Continued)

HALT CODE (OCTAL)	TEST SECTION	MEANING
106015	ANY	An interrupt to location 5 occurred without memory protect. Fix problem before proceeding.
106016	INITIALIZATION, PROGRAM AREA CHECK or TST10	Parity error in memory module 0 occurred during testing of module 0. A-register contains the data written and the B-register contains the data read. Press RUN to get the failing address.
106067	PROGRAM AREA CHECK	Program check complete. To run another pass, press RUN.
106075	ANY	Halt placed in unused memory to trap unwanted transfer of control to the location in the M-register. Fix problem before proceeding.
106077	ANY	Trap cell halt stored in locations 2 through 77_8. User must determine cause of erroneous interrupt or transfer of control to location in the M-register before proceeding.
107002	TST16	The page determination routine wrote all ones in a page and read back something other than all ones or all zeros. Fix problem and reload, or set desired maximum page number in the B-register and press RUN.

Table 4-2. Test Timing for 21MX M-Series Computers (see note)

TEST SECTION	TOTAL MEMORY SIZE INSTALLED								GREATER THAN 32K
	4K	8K	12K	16K	20K	24K	28K	32K	
TST00 Ones and Zeros	N/A	5 Sec	10 Sec	15 Sec	21 Sec	26 Sec	31 Sec	36 Sec	**
TST01 Address Parity	N/A	6 Sec	11 Sec	17 Sec	23 Sec	28 Sec	39 Sec	40 Sec	**
TST02 Marching Ones and Zeros	N/A	2 Sec	3.5 Sec	5 Sec	6.5 Sec	8 Sec	9.5 Sec	12 Sec	**
TST03 - Checkerboard	N/A	1 Sec	2 Sec	3 Sec	4 Sec	5 Sec	6 Sec	8 Sec	**
TST04 - Rows and Columns	N/A	2 Sec	4 Sec	6 Sec	9 Sec	11 Sec	13 Sec	16 Sec	**
TST05 - Disturbance	N/A	11 Sec	22 Sec	33 Sec	44 Sec	55 Sec	1 Min 6 Sec	1 Min 17 Sec	**
TST06 - Diagonal	N/A	50 Sec	1 Min 40 Sec	2 Min 30 Sec	3 Min 20 Sec	4 Min 10 Sec	5 Min	5 Min 49 Sec	**
TST07 - Relocating	N/A	10 Sec	20 Sec	30 Sec	40 Sec	50 Sec	1 Min	1 Min 10 Sec	**
TST10 - Module 0	10 Sec	10 Sec	10 Sec	10 Sec	10 Sec	10 Sec	10 Sec	10 Sec	10 Sec
TST11 - Galloping Read Recovery*	N/A	27 Min	55 Min	1 Hr 22 Min	1 Hr 50 Min	2 Hrs 17 Min	2 Hrs 44 Min	3 Hrs 13 Min	**
TST12 - Lonely Bit*	N/A	19 Min	38 Min	57 Min	1 Hr 16 Min	1 Hr 35 Min	1 Hr 54 Min	2 Hrs 13 Min	**
TST13 - Extended Instruction Group*	N/A	30 Sec	60 Sec	1 Min 30 Sec	2 Min	2 Min 30 Sec	3 Min	3 Min 30 Sec	**
TST14 - Memory Protect*	N/A	3 Sec	5 Sec	7 Sec	9 Sec	11 Sec	13 Sec	15 Sec	**
TST15 - Intervention Refresh*	N/A	***	***	***	***	***	***	***	***
TST16 Dynamic Mapping System*	N/A	**	**	**	**	**	**	**	**

*Optional Tests

**Depends on amount of memory. Execution time = $\left(\frac{\text{Memory Size Present}}{4K}\right)$ (8K execution time)

***Depends on operator response

NOTE: Times are approximate for 21MX M-Series Computers. E-Series execution time is approximately 60% of given times. In the continuous test mode (Switch-register 5 set), errors will greatly increase the above execution times.

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